L Number	Hits	Search Text	DB	Time stamp
1	1	("6248614").PN.	USPAT; US-PGPUB	2003/01/09 22:15
2	1	("20020060368").PN.	USPAT; US-PGPUB	2003/01/09 23:30
3	1	tension and (("20020060368").PN.)	USPAT; US-PGPUB	2003/01/10 00:22
4	1	wet$ and (("20020060368").PN.)	USPAT; US-PGPUB	2003/01/10 00:23
5	1	silane and (("20020060368").PN.)	USPAT; US-PGPUB	2003/01/10 00:45
6	1	(tension and (("20020060368").PN.)) and (wet$ and (("20020060368").PN.))	USPAT; US-PGPUB	2003/01/10 01:08
7	1	("6350844").PN.	USPAT; US-PGPUB	2003/01/10 01:09
8	55	(((coupling adhesion) with (silane with polyamine)) and (semiconductor integrated adj circuit)) not (@ad>20000406 @rlad>20000406)	USPAT; US-PGPUB	2003/01/10 01:10
9	115	(wet$ and (silane with polyamine) and (semiconductor integrated adj circuit)) not (@ad>20000406 @rlad>20000406)	USPAT; US-PGPUB	2003/01/10 01:14
10	1	((((coupling adhesion) with (silane with polyamine)) and (semiconductor integrated adj circuit)) not (@ad>20000406 @rlad>20000406)) and underfill$	USPAT; US-PGPUB	2003/01/10 01:11
11	3	(wet$ with silane with polyamine) and (semiconductor integrated adj circuit) not (@ad>20000406 @rlad>20000406)	USPAT; US-PGPUB	2003/01/10 01:13
12	27	(wetting and (silane with polyamine) and (semiconductor integrated adj circuit)) not (@ad>20000406 @rlad>20000406)	USPAT; US-PGPUB	2003/01/10 01:14
-	126772	surfactant	USPAT; US-PGPUB	2003/01/08 22:06
-	76553	capillary	USPAT; US-PGPUB	2003/01/08 22:06
-	478	surfactant with capillary	USPAT; US-PGPUB	2003/01/08 22:06
-	405641	semiconductor integrated adj circuit	USPAT; US-PGPUB	2003/01/08 22:07
-	48	(surfactant with capillary) and (semiconductor integrated adj circuit)	USPAT; US-PGPUB	2003/01/08 22:07
-	2751	underfil$	USPAT; US-PGPUB	2003/01/08 22:07
-	55	surfactant and underfil$ and (semiconductor integrated adj circuit)	USPAT; US-PGPUB	2003/01/08 22:08
-	387336	@ad>20000406 @rlad>20000406	USPAT; US-PGPUB	2003/01/08 22:09
-	40	(surfactant and underfil$ and (semiconductor integrated adj circuit)) not (@ad>20000406 @rlad>20000406)	USPAT; US-PGPUB	2003/01/08 22:09

-	30	((surfactant with capillary) and (semiconductor integrated adj circuit)) not (@ad>20000406 @rlad>20000406)	USPAT; US-PGPUB	2003/01/08 22:29
-	4206	glycidoxypropyltrimethoxysilane ethyltrimethoxysilane	USPAT; US-PGPUB	2003/01/08 22:41
-	34582	polyamine	USPAT; US-PGPUB	2003/01/08 22:31
-	73	(glycidoxypropyltrimethoxysilane ethyltrimethoxysilane) with polyamine	USPAT; US-PGPUB	2003/01/08 22:31
-	43	((glycidoxypropyltrimethoxysilane ethyltrimethoxysilane) with polyamine) and (semiconductor integrated adj circuit)	USPAT; US-PGPUB	2003/01/08 22:31
-	43	(((glycidoxypropyltrimethoxysilane ethyltrimethoxysilane) with polyamine) and (semiconductor integrated adj circuit)) not (@ad>20000406 @rlad>20000406)	USPAT; US-PGPUB	2003/01/08 22:31
-	49	plueddemann.in.	USPAT; US-PGPUB	2003/01/08 22:41
-	504	(glycidoxypropyltrimethoxysilane ethyltrimethoxysilane) and polyamine	USPAT; US-PGPUB	2003/01/08 22:42
-	2	((glycidoxypropyltrimethoxysilane ethyltrimethoxysilane) and polyamine) and plueddemann.in.	USPAT; US-PGPUB	2003/01/08 22:44
-	116	((glycidoxypropyltrimethoxysilane ethyltrimethoxysilane) and polyamine) and (semiconductor integrated adj circuit)	USPAT; US-PGPUB	2003/01/08 22:44
-	94	(((glycidoxypropyltrimethoxysilane ethyltrimethoxysilane) and polyamine) and (semiconductor integrated adj circuit)) not (@ad>20000406 @rlad>20000406)	USPAT; US-PGPUB	2003/01/08 22:52
-	668195	coupling adhesion	USPAT; US-PGPUB	2003/01/08 22:52
-	1443	(glycidoxypropyltrimethoxysilane ethyltrimethoxysilane) with (coupling adhesion)	USPAT; US-PGPUB	2003/01/08 22:52
-	14	underfil$ and ((glycidoxypropyltrimethoxysilane ethyltrimethoxysilane) with (coupling adhesion))	USPAT; US-PGPUB	2003/01/08 23:00
-	693	silane with polyamine	USPAT; US-PGPUB	2003/01/08 23:01
-	189	(coupling adhesion) with (silane with polyamine)	USPAT; US-PGPUB	2003/01/08 23:01
-	56	((coupling adhesion) with (silane with polyamine)) and (semiconductor integrated adj circuit)	USPAT; US-PGPUB	2003/01/08 23:01

WETTING & SURF. TENSION

DOCUMENT-IDENTIFIER: US 20020060368 A1

TITLE: Underfile process

---------- KWIC ---------

A method and apparatus for underfilling a gap between a semiconductor die or device and a substrate, where the semiconductor die or device is electrically connected to the substrate so that an active surface of the semiconductor die is facing a top surface of the substrate with the gap therebetween. A silane layer is applied to the active surface of the semiconductor die, the upper surface of the substrate, and/or both to increase the surface **tension** thereon. The increased surface **tension** thereby allows the underfill material to fill the gap via capillary action in a lesser flow time more effectively, and therefore, is more efficient than conventional underfilling methods.

[0013] The present invention relates to a method and apparatus for underfilling the gap between a bumped or raised semiconductor device and a substrate. The present invention is directed to a method and apparatus for filling the gap between a semiconductor die and a substrate using underfill material where the semiconductor die is electrically and mechanically connected to the substrate. The method and apparatus includes the use of a **wetting** agent on at least a portion of the surface of the semiconductor die forming a portion of the gap between the semiconductor die and a substrate to which it is mounted and/or a **wetting** agent on at least a portion of the substrate forming a portion of the gap to increase the surface **tension** between the underfill material and the

surface of the semiconductor die and/or the substrate. One embodiment of the present invention includes a layer of silane as a **wetting** agent on at least a portion of the active surface of the semiconductor die and/or a layer of silane on at least a portion of the upper surface of the substrate to which the semiconductor die is mounted, each layer of silane increasing the surface **tension** thereon, the increased surface **tension** allowing the underfill material to fill the gap between the semiconductor die and the substrate via capillary action forces in a lesser length of time. Various **wetting** agents may be used according to the present invention, such as glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

[0015] The method and apparatus of the present invention of the use of a **wetting** agent may be used when filling a gap between any type semiconductor device, bare or packaged, and a substrate when the semiconductor device is connected thereto.

[0017] FIG. 1 is a cross-sectional view of a portion of a semiconductor die having a **wetting** agent layer thereon and attached to a portion of a substrate having a **wetting** agent layer thereon and having an underfill material in the gap between the semiconductor die and the substrate in accordance with the present invention;

[0018] FIG. 2 is an enlarged cross-sectional view of a portion of a semiconductor die having a **wetting** agent layer thereon and a portion of a substrate having a **wetting** agent layer thereon illustrating a contact angle of the underfill material contacting a surface of the semiconductor die and a surface of the substrate in accordance with the present

invention;

[0036] In the present invention, prior to connecting the semiconductor die 12 to the circuits and/or contact pads on the upper surface 18 of the substrate 10, a **wetting** agent layer 2, such as a silane layer 2, is formed on the top surface 18 of substrate 10 and/or the active surface 20 of the semiconductor die 12. The **wetting** agent layer 2, such as a silane layer 2, can be formed thereon by any suitable spray method, brush application method, and/or a dispense method, although spraying a silane layer 2 as a **wetting** agent layer is the preferable method in order to provide a substantial uniform layer thereon. The silane layer 2 is most preferably formed as a monolayer thickness but may be formed as one or more multiple layers or formed in addition to other layers promoting a **wetting** effect on the surface of either the upper surface 18 of the substrate 10, the active surface 20 of the semiconductor die 12, or both. The silane layer 2 may be provided to the surface of the semiconductor die 12 while in its wafer form prior to or after burn-in testing, or after the wafer has been diced into multiple individual dice or an individual die. As to the substrate 10, the silane layer 2 may be provided thereon at any stage prior to the semiconductor die 12 being mounted thereto. In addition, the silane layer 2 may be comprised of any silane-based material, i.e., glycidoxypropyltrinethoxysilane (b.p. 290.degree. C.) and Ethyltrimethoxysilane (b.p. 310.degree. C.), so long as any substantial degradation thereof during any solder reflow process or curing process of the bumps 24 or any substantial degradation thereof during any burn-in and/or testing process is minimal so that the silane layer 2 promotes a sufficient **wetting** effect on the active surface 20 of the semiconductor die 12, the upper

surface 18 of the substrate 10, or both.

[0038] To promote filling of the gap 26 between the substrate 10 and semiconductor die 12, the viscosity of the underfill material 28 is controlled taking into account the flow characteristics of the underfill material 28, the material characteristics of the substrate 10, the material characteristics of the semiconductor die 12, and the size of the gap 26. By providing the silane layer 2 to the substrate 10 and the semiconductor die 12, the material characteristics of the surfaces thereof are changed so that the surface **tension** is increased. Accordingly, the underfilling of the gap 26 takes less time, allowing for a more efficient underfilling process.

[0044] .sigma. is the surface-**tension** coefficient of the underfill material; and

[0045] .theta. is the **wetting** or contact angle.

[0046] As shown in the above equation, manipulation of the contact angle .theta. can either decrease or increase the flow time t for filling the gap 2. As illustrated in drawing FIG. 2, the contact angle .theta. is the angle by which the underfill material 28 makes contact with the surface of the substrate 10 and the semiconductor die 12 via the constant capillary force driving the flow. The contact angle .theta. may be reduced by increasing the surface **tension** of the substrate 10 and semiconductor die 12, which results in a drop of flowing time. For example, according to the equation above, reducing the contact angle .theta. from 30.degree. to 10.degree. will reduce the flow time t for filling the gap 26 between the substrate and chip by 12%.

[0047] Thus, it can be appreciated that by pretreating the

surfaces of the substrate 10, the semiconductor die 12, and/or both, with a silane layer 2, as previously set forth, a **wetting** effect to the surface thereof results in an increased surface **tension**. In this manner, the contact angle .theta. is reduced, resulting in a decrease in flow time t and a more efficient and cost-effective method for underfilling the semiconductor device.

[0055] The dam 40 limits the expansion or gravitational flow of the underfill material 28 beyond the position of the dam 40. During the underfill procedure, the underfill material 28 coats and spreads out onto the surfaces of the semiconductor die 12 and substrate 10. The dam 40 prevents the spread of underfill material 28 beyond the side end 30' of the semiconductor die 12 by means of surface **tension**.

[0068] As such, while the present invention has been described in terms of certain methods and embodiments, it is not so limited, and those of ordinary skill in the art will readily recognize and appreciate that many additions, deletions and modifications to the embodiments described herein may be made without departing from the scope of the invention as hereinafter claimed. For instance, the use of a **wetting** agent can be used to enhance the flow of any type of material to fill a gap located between any substrate and any type of semiconductor device, whether a bare die type device or a packaged semiconductor device, attached thereto by any manner, such as by use of an adhesively coated tape. In the instance of a packaged semiconductor device, the **wetting** agent would be applied after packaging.

1. A semiconductor device comprising: the semiconductor device having an

active surface, at least a portion of said active surface having a **wetting** agent layer thereon.

2. The semiconductor device according to claim 1, wherein said **wetting** agent layer includes silane.

3. The semiconductor device according to claim 1, wherein said **wetting** agent layer includes at least one layer.

4. The semiconductor device according to claim 1, wherein said **wetting** agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

5. The semiconductor device according to claim 1, wherein said **wetting** agent layer reduces surface **tension** of said active surface.

6. A semiconductor assembly comprising: a semiconductor device having an active surface; a substrate having an upper surface; and a **wetting** agent layer provided on one of said active surface of said semiconductor device and said upper surface of said substrate.

7. The semiconductor assembly according to claim 6, wherein said **wetting** agent layer includes silane.

8. The semiconductor assembly according to claim 6, wherein said **wetting** agent layer includes at least one layer.

9. The semiconductor assembly according to claim 6, wherein said **wetting** agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

10. A semiconductor assembly comprising: a semiconductor device having an active surface; a substrate having an upper surface; a **wetting** agent located on a portion of one of said active surface of said

semiconductor die and said
upper surface of said substrate; and an underfill material located between
said substrate and said semiconductor device.

11. The semiconductor assembly according to claim 10, wherein said **wetting**
agent comprises silane.

12. The semiconductor assembly of claim 10, wherein said **wetting** agent
comprises at least one layer.

14. A semiconductor assembly comprising: a semiconductor device having an
active surface having at least one bond pad thereon, another surface, a first
end, a second end, a first lateral side and a second lateral side; a substrate
having an upper surface having at least one circuit thereon, a first side wall,
a second side wall, a first lateral side wall and a second lateral side wall;
at least one bump connecting said at least one bond pad on said active surface
of said semiconductor device to said at least one circuit on said upper surface
of said substrate, said at least one bump forming a gap between said
semiconductor device and said substrate; an underfill material provided
between said substrate and said semiconductor device; and a **wetting** agent
layer provided on at least a portion of one of said active surface of said
semiconductor device and said upper surface of said substrate.

15. The semiconductor assembly according to claim 14, wherein said **wetting**
agent layer comprises silane.

19. The semiconductor assembly according to claim 14, wherein said **wetting**
agent layer comprises one of glycidoxypropyltinethoxysilane and
ethyltrimethoxysilane.

20. A semiconductor assembly comprising: a semiconductor device having an active surface; a substrate having an upper surface; an underfill material provided between said substrate and said semiconductor device; and a **wetting** agent layer provided on a portion of said active surface of said semiconductor device and a portion of said upper surface of said substrate.

21. The semiconductor assembly according to claim 20, wherein said **wetting** agent layer comprises at least one layer.

22. The semiconductor assembly according to claim 20, wherein said **wetting** agent layer comprises one of silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

23. A semiconductor assembly comprising: a semiconductor device having an active surface having a plurality of bond pads thereon; a substrate having an upper surface having a plurality of circuits thereon; a plurality of bumps connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said substrate, said plurality of bumps forming a gap between said semiconductor device and said substrate; an underfill material provided between said substrate and said semiconductor device; and a **wetting** agent layer provided on said active surface of said semiconductor device and on said upper surface of said substrate.

26. A semiconductor die comprising: the semiconductor die having an active surface, at least a portion of said active surface having a **wetting** agent layer thereon.

27. The semiconductor die according to claim 26, wherein

said **wetting** agent
layer includes silane.

28. The semiconductor die according to claim 26, wherein said **wetting** agent
layer includes at least one layer.

29. The semiconductor die according to claim 26, wherein said **wetting** agent
layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

30. The semiconductor device according to claim 26, wherein said **wetting** agent
layer reduces surface **tension** of said active surface.

31. A semiconductor assembly comprising: a semiconductor die having an active
surface; a substrate having an upper surface; and a **wetting** agent layer
provided on one of said active surface of said semiconductor die and said upper
surface of said substrate.

32. The semiconductor assembly according to claim 31, wherein said **wetting**
agent layer includes silane.

33. The semiconductor assembly according to claim 31, wherein said **wetting**
agent layer includes at least one layer.

34. The semiconductor assembly according to claim 31, wherein said **wetting**
agent layer comprises one of glycidoxypropyltinethoxysilane and
ethyltrimethoxysilane.

35. A semiconductor assembly comprising: a semiconductor die having an active
surface; a substrate having an upper surface; a **wetting** agent located on a
portion of one of said active surface of said semiconductor die and said upper
surface of said substrate; and an underfill material located between said
substrate and said semiconductor die.

36. The semiconductor assembly according to claim 35, wherein said **wetting** agent comprises silane.

37. The semiconductor assembly of claim 35, wherein said **wetting** agent comprises at least one layer.

39. A semiconductor assembly comprising: a semiconductor die having an active surface having at least one bond pad thereon, another surface, a first end, a second end, a first lateral side and a second lateral side; a substrate having an upper surface having at least one circuit thereon, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall; at least one bump connecting said at least one bond pad on said active surface of said semiconductor die to said at least one circuit on said upper surface of said substrate, said at least one bump forming a gap between said semiconductor die and said substrate; an underfill material provided between said substrate and said semiconductor die; and a **wetting** agent layer provided on at least a portion of one of said active surface of said semiconductor die and said upper surface of said substrate.

40. The semiconductor assembly according to claim 39, wherein said **wetting** agent layer comprises silane.

44. The semiconductor assembly according to claim 39, wherein said **wetting** agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

45. A semiconductor assembly comprising: a semiconductor die having an active surface; a substrate having an upper surface; an underfill material provided between said substrate and said semiconductor die; and a

wetting agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate.

46. The semiconductor assembly according to claim 45, wherein said **wetting** agent layer comprises at least one layer.

47. The semiconductor assembly according to claim 45, wherein said **wetting** agent layer comprises one of silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

48. A semiconductor assembly comprising: a semiconductor die having an active surface having a plurality of bond pads thereon; a substrate having an upper surface having a plurality of circuits thereon; a plurality of bumps connecting said plurality of bond pads on said active surface of said semiconductor die to said plurality of circuits on said upper surface of said substrate, said plurality of bumps forming a gap between said semiconductor die and said substrate; an underfill material provided between said substrate and said semiconductor die; and a **wetting** agent layer provided on said active surface of said semiconductor die and on said upper surface of said substrate.

OCCURANCES OF "SILANE" IN DIUS.

DOCUMENT-IDENTIFIER: US 20020060368 A1

TITLE: Underfile process

---------- KWIC ---------

A method and apparatus for underfilling a gap between a semiconductor die or device and a substrate, where the semiconductor die or device is electrically connected to the substrate so that an active surface of the semiconductor die is facing a top surface of the substrate with the gap therebetween. A **silane** layer is applied to the active surface of the semiconductor die, the upper surface of the substrate, and/or both to increase the surface tension thereon. The increased surface tension thereby allows the underfill material to fill the gap via capillary action in a lesser flow time more effectively, and therefore, is more efficient than conventional underfilling methods.

[0013] The present invention relates to a method and apparatus for underfilling the gap between a bumped or raised semiconductor device and a substrate. The present invention is directed to a method and apparatus for filling the gap between a semiconductor die and a substrate using underfill material where the semiconductor die is electrically and mechanically connected to the substrate. The method and apparatus includes the use of a wetting agent on at least a portion of the surface of the semiconductor die forming a portion of the gap between the semiconductor die and a substrate to which it is mounted and/or a wetting agent on at least a portion of the substrate forming a portion of the gap to increase the surface tension between the underfill material and the

surface of the semiconductor die and/or the substrate. One embodiment of the present invention includes a layer of **silane** as a wetting agent on at least a portion of the active surface of the semiconductor die and/or a layer of **silane** on at least a portion of the upper surface of the substrate to which the semiconductor die is mounted, each layer of **silane** increasing the surface tension thereon, the increased surface tension allowing the underfill material to fill the gap between the semiconductor die and the substrate via capillary action forces in a lesser length of time. Various wetting agents may be used according to the present invention, such as glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

[0014] The **silane** layer may be applied to the semiconductor device and/or the substrate by a dispensing method, a brushing method, and/or a spraying method. Further, the **silane** layer may comprise at least one or more layers.

[0036] In the present invention, prior to connecting the semiconductor die 12 to the circuits and/or contact pads on the upper surface 18 of the substrate 10, a wetting agent layer 2, such as a **silane** layer 2, is formed on the top surface 18 of substrate 10 and/or the active surface 20 of the semiconductor die 12. The wetting agent layer 2, such as a **silane** layer 2, can be formed thereon by any suitable spray method, brush application method, and/or a dispense method, although spraying a **silane** layer 2 as a wetting agent layer is the preferable method in order to provide a substantial uniform layer thereon. The **silane** layer 2 is most preferably formed as a monolayer thickness but may be formed as one or more multiple layers or formed in addition to other layers

promoting a wetting effect on the surface of either the upper surface 18 of the substrate 10, the active surface 20 of the semiconductor die 12, or both. The **silane** layer 2 may be provided to the surface of the semiconductor die 12 while in its wafer form prior to or after burn-in testing, or after the wafer has been diced into multiple individual dice or an individual die. As to the substrate 10, the **silane** layer 2 may be provided thereon at any stage prior to the semiconductor die 12 being mounted thereto. In addition, the **silane** layer 2 may be comprised of any **silane**-based material, i.e., glycidoxypropyltrinethoxysilane (b.p. 290.degree. C.) and Ethyltrimethoxysilane (b.p. 310.degree. C.), so long as any substantial degradation thereof during any solder reflow process or curing process of the bumps 24 or any substantial degradation thereof during any burn-in and/or testing process is minimal so that the **silane** layer 2 promotes a sufficient wetting effect on the active surface 20 of the semiconductor die 12, the upper surface 18 of the substrate 10, or both.

[0038] To promote filling of the gap 26 between the substrate 10 and semiconductor die 12, the viscosity of the underfill material 28 is controlled taking into account the flow characteristics of the underfill material 28, the material characteristics of the substrate 10, the material characteristics of the semiconductor die 12, and the size of the gap 26. By providing the **silane** layer 2 to the substrate 10 and the semiconductor die 12, the material characteristics of the surfaces thereof are changed so that the surface tension is increased. Accordingly, the underfilling of the gap 26 takes less time, allowing for a more efficient underfilling process.

[0047] Thus, it can be appreciated that by pretreating the

surfaces of the
substrate 10, the semiconductor die 12, and/or both, with a **silane** layer 2, as
previously set forth, a wetting effect to the surface thereof results in an
increased surface tension. In this manner, the contact angle .theta. is
reduced, resulting in a decrease in flow time t and a more efficient and
cost-effective method for underfilling the semiconductor device.

[0048] Therefore, each of the embodiments hereinafter described include a
silane layer to promote faster underfilling time via capillary action, although
each embodiment may not explicitly discuss or illustrate the **silane** layer and
the effects thereof on a semiconductor die, substrate, and/or both. Rather,
the embodiments describe various methods for underfilling the gap between a
semiconductor device and a substrate. Further, it should be stated that the
present invention is not limited to the specific embodiments described below.

2. The semiconductor device according to claim 1, wherein said wetting agent
layer includes **silane**.

7. The semiconductor assembly according to claim 6, wherein said wetting agent
layer includes **silane**.

11. The semiconductor assembly according to claim 10, wherein said wetting
agent comprises **silane**.

13. The semiconductor assembly according to claim 11, wherein said **silane**
comprises any one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

15. The semiconductor assembly according to claim 14, wherein said wetting
agent layer comprises **silane**.

22. The semiconductor assembly according to claim 20, wherein said wetting agent layer comprises one of **silane,** glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

27. The semiconductor die according to claim 26, wherein said wetting agent layer includes **silane**.

32. The semiconductor assembly according to claim 31, wherein said wetting agent layer includes **silane**.

36. The semiconductor assembly according to claim 35, wherein said wetting agent comprises **silane**.

38. The semiconductor assembly according to claim 36, wherein said **silane** comprises any one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

40. The semiconductor assembly according to claim 39, wherein said wetting agent layer comprises **silane**.

47. The semiconductor assembly according to claim 45, wherein said wetting agent layer comprises one of **silane,** glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

OCCURANCES of "WETTING" in DIMS

DOCUMENT-IDENTIFIER: US 20020060368 A1

TITLE: Underfile process

---------- KWIC ---------

[0013] The present invention relates to a method and apparatus for underfilling the gap between a bumped or raised semiconductor device and a substrate. The present invention is directed to a method and apparatus for filling the gap between a semiconductor die and a substrate using underfill material where the semiconductor die is electrically and mechanically connected to the substrate. The method and apparatus includes the use of a **wetting** agent on at least a portion of the surface of the semiconductor die forming a portion of the gap between the semiconductor die and a substrate to which it is mounted and/or a **wetting** agent on at least a portion of the substrate forming a portion of the gap to increase the surface tension between the underfill material and the surface of the semiconductor die and/or the substrate. One embodiment of the present invention includes a layer of silane as a **wetting** agent on at least a portion of the active surface of the semiconductor die and/or a layer of silane on at least a portion of the upper surface of the substrate to which the semiconductor die is mounted, each layer of silane increasing the surface tension thereon, the increased surface tension allowing the underfill material to fill the gap between the semiconductor die and the substrate via capillary action forces in a lesser length of time. Various **wetting** agents may be used according to the present invention, such as glycidoxypropyltinethoxysilane and

ethyltrimethoxysilane.

[0015] The method and apparatus of the present invention of the use of a **wetting** agent may be used when filling a gap between any type semiconductor device, bare or packaged, and a substrate when the semiconductor device is connected thereto.

[0017] FIG. 1 is a cross-sectional view of a portion of a semiconductor die having a **wetting** agent layer thereon and attached to a portion of a substrate having a **wetting** agent layer thereon and having an underfill material in the gap between the semiconductor die and the substrate in accordance with the present invention;

[0018] FIG. 2 is an enlarged cross-sectional view of a portion of a semiconductor die having a **wetting** agent layer thereon and a portion of a substrate having a **wetting** agent layer thereon illustrating a contact angle of the underfill material contacting a surface of the semiconductor die and a surface of the substrate in accordance with the present invention;

[0036] In the present invention, prior to connecting the semiconductor die 12 to the circuits and/or contact pads on the upper surface 18 of the substrate 10, a **wetting** agent layer 2, such as a silane layer 2, is formed on the top surface 18 of substrate 10 and/or the active surface 20 of the semiconductor die 12. The **wetting** agent layer 2, such as a silane layer 2, can be formed thereon by any suitable spray method, brush application method, and/or a dispense method, although spraying a silane layer 2 as a **wetting** agent layer is the preferable method in order to provide a substantial uniform layer thereon.

The silane layer 2 is most preferably formed as a monolayer thickness but may be formed as one or more multiple layers or formed in addition to other layers promoting a **wetting** effect on the surface of either the upper surface 18 of the substrate 10, the active surface 20 of the semiconductor die 12, or both. The silane layer 2 may be provided to the surface of the semiconductor die 12 while in its wafer form prior to or after burn-in testing, or after the wafer has been diced into multiple individual dice or an individual die. As to the substrate 10, the silane layer 2 may be provided thereon at any stage prior to the semiconductor die 12 being mounted thereto. In addition, the silane layer 2 may be comprised of any silane-based material, i.e., glycidoxypropyltrinethoxysilane (b.p. 290.degree. C.) and Ethyltrimethoxysilane (b.p. 310.degree. C.), so long as any substantial degradation thereof during any solder reflow process or curing process of the bumps 24 or any substantial degradation thereof during any burn-in and/or testing process is minimal so that the silane layer 2 promotes a sufficient **wetting** effect on the active surface 20 of the semiconductor die 12, the upper surface 18 of the substrate 10, or both.

[0045] .theta. is the **wetting** or contact angle.

[0047] Thus, it can be appreciated that by pretreating the surfaces of the substrate 10, the semiconductor die 12, and/or both, with a silane layer 2, as previously set forth, a **wetting** effect to the surface thereof results in an increased surface tension. In this manner, the contact angle .theta. is reduced, resulting in a decrease in flow time t and a more efficient and cost-effective method for underfilling the semiconductor device.

[0068] As such, while the present invention has been

described in terms of certain methods and embodiments, it is not so limited, and those of ordinary skill in the art will readily recognize and appreciate that many additions, deletions and modifications to the embodiments described herein may be made without departing from the scope of the invention as hereinafter claimed. For instance, the use of a **wetting** agent can be used to enhance the flow of any type of material to fill a gap located between any substrate and any type of semiconductor device, whether a bare die type device or a packaged semiconductor device, attached thereto by any manner, such as by use of an adhesively coated tape. In the instance of a packaged semiconductor device, the **wetting** agent would be applied after packaging.

1. A semiconductor device comprising: the semiconductor device having an active surface, at least a portion of said active surface having a **wetting** agent layer thereon.

2. The semiconductor device according to claim 1, wherein said **wetting** agent layer includes silane.

3. The semiconductor device according to claim 1, wherein said **wetting** agent layer includes at least one layer.

4. The semiconductor device according to claim 1, wherein said **wetting** agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

5. The semiconductor device according to claim 1, wherein said **wetting** agent layer reduces surface tension of said active surface.

6. A semiconductor assembly comprising: a semiconductor device having an active surface; a substrate having an upper surface; and a

wetting agent
layer provided on one of said active surface of said semiconductor device and
said upper surface of said substrate.

7. The semiconductor assembly according to claim 6, wherein said **wetting** agent
layer includes silane.

8. The semiconductor assembly according to claim 6, wherein said **wetting** agent
layer includes at least one layer.

9. The semiconductor assembly according to claim 6, wherein said **wetting** agent
layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

10. A semiconductor assembly comprising: a semiconductor device having an
active surface; a substrate having an upper surface; a **wetting** agent located
on a portion of one of said active surface of said semiconductor die and said
upper surface of said substrate; and an underfill material located between
said substrate and said semiconductor device.

11. The semiconductor assembly according to claim 10, wherein said **wetting**
agent comprises silane.

12. The semiconductor assembly of claim 10, wherein said **wetting** agent
comprises at least one layer.

14. A semiconductor assembly comprising: a semiconductor device having an
active surface having at least one bond pad thereon, another surface, a first
end, a second end, a first lateral side and a second lateral side; a substrate
having an upper surface having at least one circuit thereon, a first side wall,
a second side wall, a first lateral side wall and a second lateral side wall;
at least one bump connecting said at least one bond pad on

said active surface
of said semiconductor device to said at least one circuit on said upper surface
of said substrate, said at least one bump forming a gap between said
semiconductor device and said substrate; an underfill material provided
between said substrate and said semiconductor device; and a **wetting** agent
layer provided on at least a portion of one of said active surface of said
semiconductor device and said upper surface of said substrate.

15. The semiconductor assembly according to claim 14, wherein said **wetting**
agent layer comprises silane.

19. The semiconductor assembly according to claim 14, wherein said **wetting**
agent layer comprises one of glycidoxypropyltinethoxysilane and
ethyltrimethoxysilane.

20. A semiconductor assembly comprising: a semiconductor device having an
active surface; a substrate having an upper surface; an underfill material
provided between said substrate and said semiconductor device; and a **wetting**
agent layer provided on a portion of said active surface of said semiconductor
device and a portion of said upper surface of said substrate.

21. The semiconductor assembly according to claim 20, wherein said **wetting**
agent layer comprises at least one layer.

22. The semiconductor assembly according to claim 20, wherein said **wetting**
agent layer comprises one of silane,
glycidoxypropyltinethoxysilane and
ethyltrimethoxysilane.

23. A semiconductor assembly comprising: a semiconductor device having an
active surface having a plurality of bond pads thereon; a

substrate having an upper surface having a plurality of circuits thereon; a plurality of bumps connecting said plurality of bond pads on said active surface of said semiconductor device to said plurality of circuits on said upper surface of said substrate, said plurality of bumps forming a gap between said semiconductor device and said substrate; an underfill material provided between said substrate and said semiconductor device; and a **wetting** agent layer provided on said active surface of said semiconductor device and on said upper surface of said substrate.

26. A semiconductor die comprising: the semiconductor die having an active surface, at least a portion of said active surface having a **wetting** agent layer thereon.

27. The semiconductor die according to claim 26, wherein said **wetting** agent layer includes silane.

28. The semiconductor die according to claim 26, wherein said **wetting** agent layer includes at least one layer.

29. The semiconductor die according to claim 26, wherein said **wetting** agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

30. The semiconductor device according to claim 26, wherein said **wetting** agent layer reduces surface tension of said active surface.

31. A semiconductor assembly comprising: a semiconductor die having an active surface; a substrate having an upper surface; and a **wetting** agent layer provided on one of said active surface of said semiconductor die and said upper surface of said substrate.

32. The semiconductor assembly according to claim 31, wherein said **wetting** agent layer includes silane.

33. The semiconductor assembly according to claim 31, wherein said **wetting** agent layer includes at least one layer.

34. The semiconductor assembly according to claim 31, wherein said **wetting** agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

35. A semiconductor assembly comprising: a semiconductor die having an active surface; a substrate having an upper surface; a **wetting** agent located on a portion of one of said active surface of said semiconductor die and said upper surface of said substrate; and an underfill material located between said substrate and said semiconductor die.

36. The semiconductor assembly according to claim 35, wherein said **wetting** agent comprises silane.

37. The semiconductor assembly of claim 35, wherein said **wetting** agent comprises at least one layer.

39. A semiconductor assembly comprising: a semiconductor die having an active surface having at least one bond pad thereon, another surface, a first end, a second end, a first lateral side and a second lateral side; a substrate having an upper surface having at least one circuit thereon, a first side wall, a second side wall, a first lateral side wall and a second lateral side wall; at least one bump connecting said at least one bond pad on said active surface of said semiconductor die to said at least one circuit on said upper surface of

said substrate, said at least one bump forming a gap between said semiconductor die and said substrate; an underfill material provided between said substrate and said semiconductor die; and a **wetting** agent layer provided on at least a portion of one of said active surface of said semiconductor die and said upper surface of said substrate.

40. The semiconductor assembly according to claim 39, wherein said **wetting** agent layer comprises silane.

44. The semiconductor assembly according to claim 39, wherein said **wetting** agent layer comprises one of glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

45. A semiconductor assembly comprising: a semiconductor die having an active surface; a substrate having an upper surface; an underfill material provided between said substrate and said semiconductor die; and a **wetting** agent layer provided on a portion of said active surface of said semiconductor die and a portion of said upper surface of said substrate.

46. The semiconductor assembly according to claim 45, wherein said **wetting** agent layer comprises at least one layer.

47. The semiconductor assembly according to claim 45, wherein said **wetting** agent layer comprises one of silane, glycidoxypropyltinethoxysilane and ethyltrimethoxysilane.

48. A semiconductor assembly comprising: a semiconductor die having an active surface having a plurality of bond pads thereon; a substrate having an upper surface having a plurality of circuits thereon; a plurality of bumps connecting said plurality of bond pads on said active surface

of said
semiconductor die to said plurality of circuits on said upper surface of said
substrate, said plurality of bumps forming a gap between said semiconductor die
and said substrate; an underfill material provided between said substrate and
said semiconductor die; and a **wetting** agent layer provided on said active
surface of said semiconductor die and on said upper surface of said substrate.